An Active Diode Full-Wave Charge Pump for Low Acceleration Infrastructure-Based Non-Periodic Vibration Energy Harvesting

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***Abstract*— An active diode IC-based full-wave charge pump is presented. It interfaces to a vibration harvester designed for low acceleration non-periodic bridge vibrations. The charge pump's unique architecture uses only two comparators to switch the charge pump's eight stages. This architecture reduces power and allows for a novel passive diode switching technique that also enables a reduction in the turn-on voltage. This switching technique initially functions based only on the AC input without a DC supply. This architecture is used to enable cold start-up using the charge pump's external 100 μF capacitors. These large capacitors create a stable power supply for start-up from one low voltage AC input based off of bridge vibrations that are random and infrequent. Its rectification circuitry is fabricated in 180 nm CMOS on a 1.2 mm^2 die. The circuit inputs, generated using a shaker table, are periodic sine-waves or non-periodic mechanical frequency up-converted vibration harvester outputs. Measurements show that the diode drop reduction allows cold start-up and boosting to >1.5 V with low power (∼8.5 μW) non-periodic harvester outputs or 220 mV open circuit voltage periodic (∼100 Hz) inputs. This IC demonstrates ∼50% efficiency with an up-conversion-based harvester and ∼1 μW active power dissipation.**

***Index Terms*— Frequency up-conversion, PFIG, vibration harvesting, structural health monitoring, charge pump, sub-threshold, CMOS, interface circuit, comparator, start-up.**

I. Introduction

SENSORS can analyze a bridge's structural integrity [1], [2]. These sensors can obtain information that may quickly identify necessary repairs on a bridge. However, underneath a large suspension bridge [3]–[5] battery replacement proves difficult and solar power can be limited and even unavailable. This motivates harvesting new types of power sources from the environment. Harvesting energy in every possible environment requires innovative harvesting methods and circuit interfaces. The presented research focuses on an interface circuit for harvesting vibrations from a bridge due to passing vehicles. These low acceleration vibrations are non-periodic and sometimes absent for extended periods.

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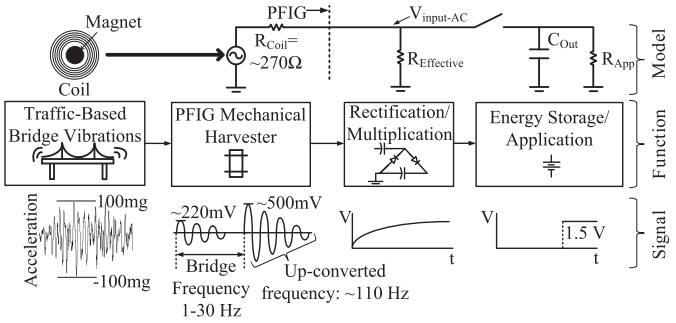

Fig. 1. Diagram of the energy harvesting system. In the top part of the diagram, a simple voltage divider represents the connection between the PFIG and charge pump.

To harvest vibrations from a bridge, a broadband vibration harvester is necessary. Broadband vibration harvesters capture energy from a range of frequencies. One approach is to simultaneously rectify multiple frequencies from a piezoelectric disk [6]. Another approach is to tune a harvester's resonant frequency, but this consumes too much power [7], [8]. The interface circuit presented here was specifically designed for and is tested with the electromagnetic Parametric Frequency Increased Generator (PFIG) [3]–[5], [9]–[11]. Extensive pictures and description of the PFIG are also included in [12] and [13]. It can harvest traffic-induced broadband frequencies and accelerations on a bridge (e.g. 30-100 mg (1 g = 9.81 m/s^2) between 1-30 Hz [3]). It uses mechanical frequency up-conversion to generate a decaying sine-wave output at >100 Hz [14] (Fig. 1). A more detailed description of the PFIG and its testing is given in Sections II and III. In a year-long bridge study [5], a single FIG output regularly exceeded 10 μW for ∼20 seconds. Nights and weekends generated little power [4], [5], emphasizing the need for circuit start-up.

The FIG output presents the challenge that one low voltage low power AC output must frequently cold start-up the interface circuit. This will require boosting and must be done without transformers or a pre-charged supply. Also, it must allow an application R_{App} to be supplied at a specific voltage (Fig. 1). Finally, the non-periodic and sometimes infrequent inputs motivate charging large off-chip (e.g. 100 μF) capacitors from cold start to maintain circuit stability.

The classic Cockcroft-Walton (CW) charge pump (Fig. 2) allows start-up and boosting [15]. It is used as the building block of the presented architecture. Passive [4] and active [16], [17] CW charge pumps regularly use large capacitors ranging from 10-220 μF. This classic CW charge

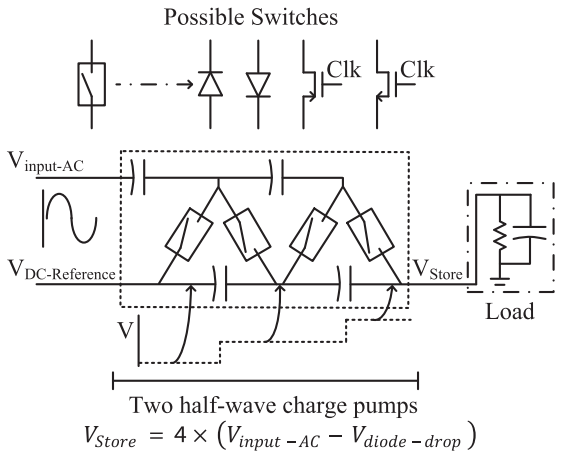

Fig. 2. A two stage passive half-wave Cockcroft-Walton charge pump interface circuit with equations describing maximum boosting.

pump has an AC input and a DC reference. The CW charge pump boosts from the DC reference voltage to an output DC storage voltage (V_{Store}). The switches that boost the charge pump can be passive diodes in either direction or active NMOS (n-channel MOSFET) or PMOS (p-channel MOSFET) diodes/switches. Even purely mechanical switches (actuated by vibrations) can be used in charge pumps [18] or rectifiers [19]. Active NMOS or PMOS switches need a DC power supply to generate a switching signal at their gates. Both MOSFETS and diodes have a technology dependent turn-on voltage that must be overcome to allow charge flow. In MOSFETs this is the threshold voltage (V_{th}). The presented circuit research reduces current and turn-on voltages with its unique IC design using only two comparators, inverters, and buffers to switch an entire CW charge pump. Additionally, the comparator and inverter/buffer implementation are well suited to low voltages and create a unique passive switching technique.

Advances in wireless sensors and microprocessors have reduced power and voltage requirements [20], [21]. Some sensors require <6 nWs [22]–[24]. However, low-power microprocessors may still require ∼300 μW at ∼1.8 V [21]. An on-chip battery [25] or capacitor may be sufficient to supply ∼nW sensors, but a microprocessor requires off-chip storage (e.g. a ∼100 μF capacitor). External storage is necessary because the harvested output can be infrequent (e.g. on a bridge) and power limited (∼5-10 μW). Nevertheless the power supply must be stable. The presented circuit could be part of a wireless multi-harvester system used to supply a microprocessor regularly in sleep mode [7], [21], [26]. Here an IC allows the use of design techniques and technology characteristics, unavailable in discrete electronics, to meet system requirements.

The presented charge pump circuit connects to the coil in the PFIG (an electromagnetic harvester). This coil has negligible inductance or capacitance and is modeled as an AC source and resistor. For comparison, research into interface circuits for piezoelectric vibration harvesters often focuses on manipulating the non-negligible harvester capacitive element for high efficiency [27]–[32]. Additionally, research on start-up for piezoelectric harvester interface circuits can focus on reducing the required start-up power [33] or demonstrating start-up under real-world conditions (e.g. using vibration data from a tram [34]). Charge pumps can also be used with low voltage piezoelectric harvesters. An inductor in these charge pumps optimizes matching with the piezoelectric harvester and its capacitive element [35].

Previous PFIG interface circuits for low-voltage inputs used half-wave CW charge pumps made from off-chip capacitors (10 μF) with and without transformers [3]–[5]. Charge pumps enable boosting and start-up as the input is harvested. At the same time, the input is used as a clock to switch the diodes. The PFIG's passive charge pumps [3]–[5] used Schottky diodes with a ∼180 mV turn-on voltage. The reduced turn-on voltage of the Schottky diodes in a charge pump allowed start-up with a PFIG's ∼300 mV peak voltage and 5-10% efficiency. In other research Schottky diodes have also been used to create a supply with a dual output vibration harvester. One harvester output creates a supply while the other output is actively harvested. However, this means only one of two outputs is harvested [36]. This motivates other boosting solutions.

Transformers can boost a harvester's AC signal to overcome diode drops, but they have disadvantages. To begin with they can be large [3]. Also, while an interface circuit matched to a low impedance (3-4 Ω) electromagnetic harvester can have high efficiencies (65%) [37]–[39], circuits that interface to a high impedance (∼300 Ω) low frequency FIG output have reduced efficiency (∼38%) [3]–[5]. This is due to the efficiency reduction in the transformer. Additionally, a harvester's power may be limited by the design requirement that its impedance match to the input impedance of a specific transformer [3].

Several circuit techniques reduce turn-on voltage for vibration harvester inputs that are >∼1 μA. A passive negative voltage converter (NVC), similar to a gate-cross-coupled rectifier [40], converts the negative portion of an AC input positive to simplify full rectification in a subsequent stage [41]–[45]. Once the NVC's input overcomes the technology's V_{th}, its voltage drop is ∼0 V. However, the minimum voltage for NVC functionality is still V_{th} dependent (e.g. ∼380 mV for 0.35 μm CMOS [43] or ∼300 mV for 65 nm CMOS [45]).

Active diodes can also reduce turn-on voltages. The basic concept behind an active diode is that a NMOS or PMOS device is switched similar to a passive diode to reduce the device's turn-on voltage to allow current flow. These devices could be switched by a comparator or clock signal. Active AC-DC solutions that boost and rectify improve efficiency, but they have difficulty with cold start-up. For example, active fully integrated switched capacitor/charge pump ICs have been built [44] that boost vibration harvester outputs, but they need a 0.8 V pre-charged supply to generate a clock. A rectifier-free AC-DC LC boost converter has been investigated, but it still needs a pre-charged supply [46]. Conversely, AC-DC LC boost converters don't always need a clock or pre-charge supply for start-up, but they still need to rectify. This rectification still depends on the diode's turn-on voltage [47]–[50].

A brief discussion of rectification research for both radio frequency (RF) and even thermal harvesting circuits is

also relevant. This is especially true when similar techniques are or could be used in vibration harvesting interface circuits to reduce a diode's turn-on voltage. AC-DC RF harvesters use half-wave [51], [52] and even full-wave charge pumps [53]. RF research regularly focuses on the choice of interface circuit (e.g. a Dickson [54] or a Cockcroft charge pump) [55]. The key difference between these RF harvesting circuits and active diode charge pumps is that the active diode charge pumps use comparators to reduce the turn-on voltage at higher currents (e.g. $\geq$10 μA). Often RF harvesting circuits are designed for very low current ($\sim$nA) inputs. This low current reduces the turn-on voltage in the diodes [51]. This is because the diode turn-on voltage reduces by $\sim$100 mV for every decade of current from $\sim\mu$A to $\sim$pA [52]. A similar response is observed in vibration harvesting circuits when charging integrated capacitors $\sim$nF [56], [57]. Techniques in RF circuits such as floating gate capacitors can reduce turn-on voltages when using a large 10 μF load [52]. However, the charge on these floating gate capacitors cannot be maintained for decades [52]. This is needed for long-term bridge harvesting. Charging $>$10 μF capacitors [5], [52] from a low voltage energy harvester remains a challenge.

There are multiple techniques to enable and start-up DC-DC converters. Some techniques indirectly use rectification, or they use external vibrations. For example, a vibration activated external switch can enable start-up in low voltage DC-DC harvesters [58]. Other research using charge pumps [59] or a charge pump and LC Boost converter [60], [61] use low voltage DC inputs (70-120 mV) to create a clock which allows boosting in a charge pump similar to the basic Dickson charge pump [54] with $\sim$pF-nF integrated capacitors. In DC-DC thermal harvesting research extensive consideration is given to switches or Schmitt triggers [60]–[62] that allow lower current integrated capacitor charging (i.e. $\sim$pA-nA) at one voltage while allowing higher current load (i.e. $\sim$mA) at another voltage. The presented research describes a very different type of application in which large off-chip (100 μF) capacitors are charged from start-up with a non-periodic AC signal. This means that there is not the turn-on voltage reduction associated with lowered currents and a constant harvesting source is unavailable.

The presented research builds on the concept of a full-wave active diode charge pump using large 100-200 μF capacitors. Single and multiple stage discrete active diode charge pumps have been built [16], [17], [63] for vibration harvesters. The large capacitors are needed to optimize efficiency by not limiting current and allowing for stable charging [64]. Well characterized efficiencies exceed 70% for higher power inputs at $>$1 kHz. With a comparator for every active diode, power consumption is $\sim$6 μW [16], [17]. Using integrated circuits rather than discrete components provides many advantages. These advantages are a significant reduction in start-up turn-on voltage, a power consumption reduction, and an architecture that can be tailored to and tested with lower voltage non-periodic inputs.

Recent research shows that the minimum peak AC input voltage required for cold start-up in a harvesting system charging a load requiring moderate to high currents is between

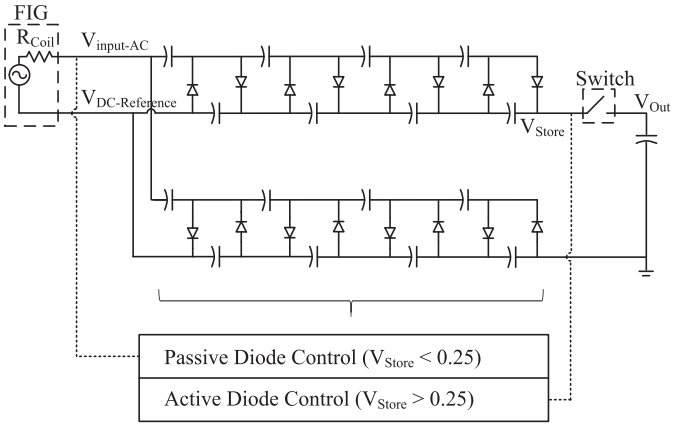

Fig. 3. The full-wave Cockcroft-Walton charge pump architecture in the presented research. The passive/active diode control is shown.

380 mV to 600 mV [16], [17], [63], [65]–[70]. The presented research uses a full-wave charge pump (Fig. 3) containing 100 μF capacitors and rectification circuity built using 180 nm CMOS to boost, rectify, and allow start-up with a 220 mV AC input. This low voltage start-up is enabled using a novel leakage-based technique. In this technique, initially only the AC input, without a DC supply, reduces the turn-on voltage. Once $\sim$250 mV is built-up on the charge pump output, the active diode operation through multiple regions of functioning is analyzed as the charge pump output rises to over 1 V.

Additionally, the presented research describes a novel analysis of a low power trigger/switch. Current energy harvesting research continues to investigate ultra-low power triggers [71] or Schmitt triggers [62] that allow current flow at a specific DC voltage [60]. The switch used in this research employs a mode selector architecture [72], [73]. As shown here the mode selector architecture can allow for an adjustable DC trigger voltage. This adjustability allows investigation into charging a load at different voltages from the charge pump.

Finally, the experimental data presented here addresses the novel system challenges assessing an interface circuit built for low acceleration infrastructure-based vibrations harvested by a mechanical up-conversion-based harvester. This type of energy harvester produces an output similar to a decaying sine-wave [3]–[5] when actuated by vibrations $<$100 mg at frequencies $<$10 Hz. However, it is difficult to understand the full circuit performance with non-periodic decaying sine-wave inputs. To address this concern the mechanical energy harvester is disassembled to allow a sine-wave output to be produced. This allows a unique comparison between the charge pump interface circuit's characteristics with a sine-wave input versus an up-conversion-based decaying sine-wave input using the same electromagnetic coil and magnet.

II. System Description

A. The Parametric Frequency Increased Generator (PFIG)

The PFIG vibration energy harvester, described in Fig. 4a, is 7.3 cm tall with a diameter of 3.3 cm [4], [13]. To enable frequency up-conversion, a large tungsten carbide inertial mass with a diameter of 2.54 cm snaps back and forth between

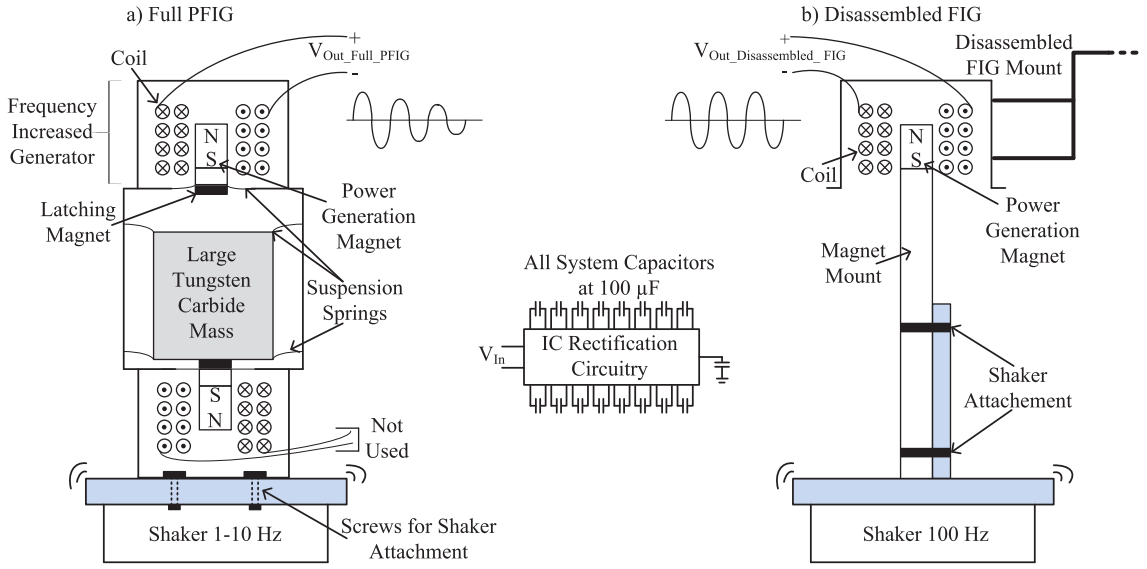

Fig. 4. a) Mechanical up-conversion is illustrated with the PFIG [3], [4]. b) A rod is attached to a shaker and used to mount a power generation magnet. The shaker oscillates the magnet through a PFIG coil at 100 Hz to produce a sine-wave. The input into the circuit is shown in the middle of the diagram.

latching magnets on two suspension springs. When the mass is released, each spring oscillates at an up-converted frequency. A power generation magnet on top of each spring produces a decaying sine-wave voltage when it oscillates within a copper coil. The portion of the PFIG containing the copper coil and power generation magnet is referred to as a frequency increased generator (i.e. a FIG).

The up-converted PFIG output is a decaying sine-wave voltage oscillating at ∼100-110 Hz. The PFIG allows low frequency low acceleration vibrations to be up-converted into high frequency high acceleration decaying sine-waves. For example the maximum acceleration of the FIG suspension spring can be calculated using PFIG characteristics [4] such as the FIG suspension spring constant and the power generation magnet mass. With these PFIG characteristics, it can be understood that the ∼50 mg acceleration that detaches the large tungsten carbide inertial mass might lead to a maximum displacement of <0.1 mm and a corresponding maximum acceleration between 5-10 g at the FIG suspension spring. The PFIG has peak open circuit outputs decreasing from ∼450 to ∼220 mV with a 200-300 Ω output impedance. The challenge for the interface circuit is how to harvest, boost and rectify this output signal. Additionally, Section III will describe how the PFIG is disassembled (Fig. 4b) so that the interface circuit's response to a sine-wave can also be studied.

B. ×16 Full-Wave Charge Pump Architecture

A charge pump, the basic architecture used in the presented circuit, is the best way to boost and start-up with an AC input because it enables low voltage start-up and high efficiency boosting. The goal of this circuit is to achieve a ∼1.5 V output to store charge in 100 μF capacitors. In order to achieve the desired 1.5 V DC output at optimal efficiency, a maximum output voltage of twice that is needed, i.e. $V_{Out} > 3$ V [74]. The number of charge pump stages were chosen based on

$$V_{outCW} = 2 \times n \times (V_{Peak} - V_{diode-drop}) \quad (1)$$

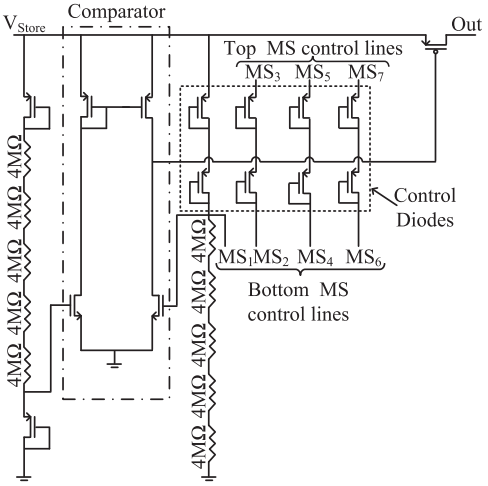

Fig. 5. The mode selector design that allows current to pass when an adjustable voltage is reached.

where V_{outCW} is the maximum voltage of an n-stage CW charge pump to rectify and boost a decaying sine-wave with peak voltage, V_{peak}. $V_{diode-drop}$ is the diode drop (either active or passive). Assuming a 220 mV input and an acitve $V_{diode-drop}$ of ∼15-20 mV from simulation, the eight-stage design with ×2 boosting in each stage maximizes efficiency. Since the PFIG output is similar to a decaying sine-wave, a 220 mV peak can be a typical peak in a PFIG signal with ∼400 mV maximum peak.

Fig. 3 shows the charge pump architecture used in the presented research. It is formed from two half-wave charge pumps with four stages each. As seen in Fig. 2 the diodes can be oriented in either direction to allow harvesting and boosting of positive and negative voltages. The DC-references of two of these charge pumps can be connected to produce the architecture seen in Fig. 3 [16], [17], [47]. A common ground for a multi-harvester system can be used by connecting the bottom charge pump output to ground. A switch separates the main charge pump from a load capacitance. All charge

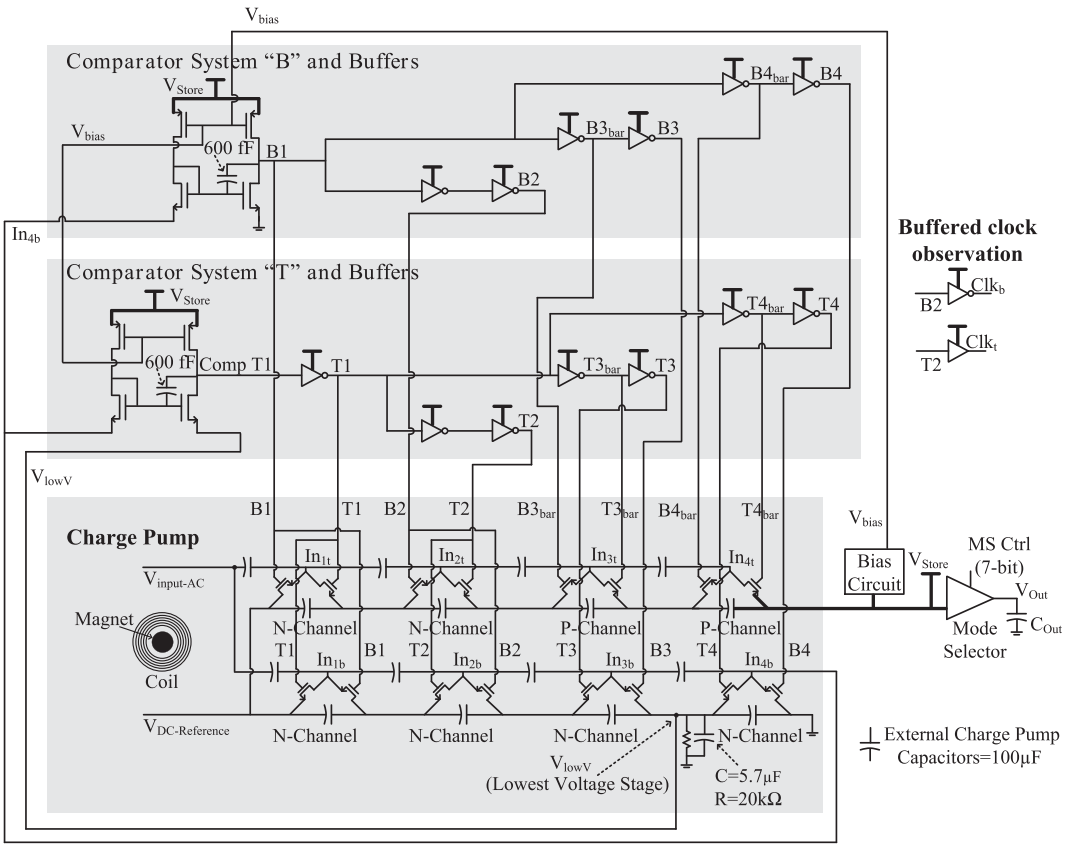

Fig. 6. The expanded full-wave charge pump presented here with detailed connections. The individual active diodes, comparators, inverters, and mode selector are shown. Its input is a magnet oscillating through a coil.

pump capacitors and the load capacitance are 100 μF. The potential application R_{App} attached on Fig. 1 could use line and load regulation to protect the output voltage, but this is not considered here. As will be explained in Section II. D, comparators sense the inputs into the bottom active diodes, and they drive all of the active diodes in the charge pump through inverters and buffers using both active and novel passive functioning.

C. Mode Selector Switch and Charge Pump Loading

An adjustable mode selector (Fig. 5) placed at the output of the charge pump (V_{Store}) allows the voltage where V_{Store} is loaded to be evaluated and adjusted to maximize start-up. Similar to RF implementations [72], [73], the mode selector lets current pass when a specific voltage is reached by creating a crossing point between the inputs into a low power comparator. This crossing point is controlled by the non-linear behavior of diodes in the input lines. RF mode selectors use five 5 MΩ resistors in their input lines [72], [73]. Here, low power is maintained by using five 4 MΩ resistors created from 1 μm width high resistance polysilicon forming ~57 μm × ~72 μm rectangles (Fig. 7). Seven control lines for this mode selector are shown in Fig. 5. By connecting or disconnecting these lines, diodes are added or subtracted to adjust the crossing point of the inputs into the comparator to allow charging into V_{Out} between 0.8 V and 1.5 V. For example, if V_{Store} and MS3 are connected while MS1 and MS2 are connected, V_{Out} charges at a voltage below 1.5 V.

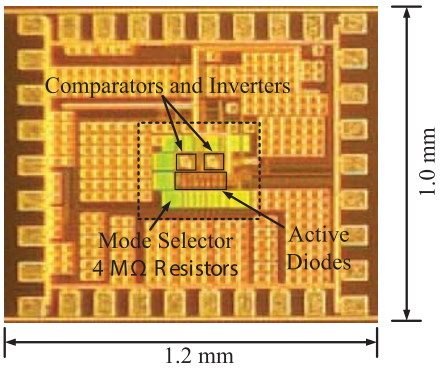

Fig. 7. The 1 mm × 1.2 mm CMOS die. The active diode region is indicated by a dashed square containing the 4 MΩ mode selector resistors, active diodes, comparators, and inverters.

D. Active Diode Control Circuitry Using Two Comparators

Fig. 6 shows the active diode full-wave charge pump with a detailed description of the electronics. It is fabricated in 180 nm CMOS on a 1.2 mm^2 die (Fig. 7). This section describes its architecture and how its design choices affect operation in saturation. Section III describes the effect of these design choices from the 0 V sub-threshold start-up.

As in Fig. 2, the input in Fig. 6 is harvested at the same time it is used as a clock to turn on and off the diodes to allow boosting in the charge pump. There are eight stages in the modified CW charge pump that boost in the negative and positive direction. The charge pump's output (V_{Store}) supplies the active components (comparators, inverters, bias, and mode

selector). Similar to other charge pump designs [3], [16], [17], capacitors are large (10-200 μF) to achieve high efficiency.

Two comparators [42], [75] on the lowest voltage stage (the bottom of the negative charge pump) switch the entire system's active diodes through inverters and buffers. The input signal travels through all of the capacitors to switch this differential to single ended common gate comparator (Fig. 6). The input into the lowest voltage stage comparators is In_{4b}. The DC output at the bottom stage of the charge pump is V_{lowV}. In saturation these comparators and their placement on the lowest voltage stage are well suited for a low voltage input near ground. For example, when In_{4b} exceeds V_{lowV} in the 2^{nd} comparator in Fig. 6, the voltage on the gates of the NMOS devices in the comparator rises. This pulls the comparator's output to V_{lowV}. With this comparator, low voltages near ground switch the comparator without needing to overcome the V_{th} at a gate. To represent the comparator outputs, signals Clk_b and Clk_t are sent to the pads, after buffering, for observation (Fig. 6). The comparator's PMOS loads are biased by V_{Bias} [75] (also sent to a pad for observation). The V_{Bias} turns on when V_{Store} is equal to V_{th} and stays one V_{th} below V_{Store}. If this comparator were used on a higher voltage stage, the comparator would pull its output down to a voltage that is higher than V_{lowV}. This voltage may not be low enough to drive the inverter/buffer chain. Section III discusses how the comparator placement aids passive start-up switching. It is worth noting that the comparator's role and functioning is different than what is described here when the architecture is used for start-up from 0 V as described in Section III.

The top two stages of the positive charge pump are comprised of PMOS devices. The rest of the stages use NMOS devices. For comparison, discrete charge pumps use both NMOS and PMOS devices in every stage to both align the sources to the DC referenced input and form passive start-up diodes using bulk connections [16], [17], [63]. PMOS devices on the top stages rather than NMOS devices have the potential for greater harvested current flow. For example, if V_{Store} is $\sim$1 V, a $\sim$1 V difference will overcome the V_{th} in the PMOS devices as their gate is pulled to ground. If NMOS devices are used on the top stage, turning an active diode high to V_{Store} may only allow $\sim$200-300 mV to overcome the $>$500 mV NMOS V_{th}. The presented charge pump can start-up with passive switching and does not need passive diodes shorted across its active diodes.

After the comparators, the inverter/buffer chain switches the other stages. Both the NMOS and PMOS active diodes have L = 180 nm and W = 150 μm (15 fingers of 10 μm). The high W/L ratio was chosen to maximize current flow for a given V_{gs} in saturation (and sub-threshold), but this was balanced with noise on the comparator outputs. With large active diodes in saturation, the comparator can turn on the inverters before it is fully on. This in turn loads the harvester output creating feedback in the system, and the corresponding noise increases active power. It is reduced by adding a 600 fF compensation capacitor to the comparator (Fig. 6). To verify circuit operation the buffered top and bottom comparator clocks are sent out to pads (Fig. 6). ESD diodes are used on the the pads to provide basic overvoltage protection.

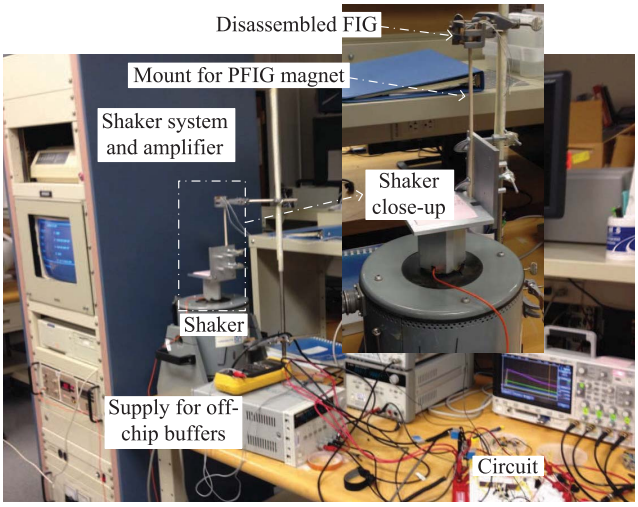

Fig. 8. Setup for testing the circuit with a $\sim$100 Hz sine wave. A close-up of the shaker and disassembled FIG are shown.

III. Circuit Results and Discussion

A. Charge Pump Evaluation Method

The charge pump interface was tested with a PFIG output. However, to illustrate circuit functioning and compare start-up to other research, the presented circuit can also be tested with a periodic sine-wave. Disassembling a PFIG and using a shaker table to oscillate a PFIG-based magnet through a PFIG coil at 100 Hz generates a sine-wave (Fig. 4b). This allows easy comparison between sine-wave inputs and non-periodic inputs generated by the PFIG (Fig. 4a). For example, sine-waves with maximum peak inputs of 220 mV, 280 mV, and 350 mV were tested with the charge pump interface. These values were chosen because they correspond to the maximum peaks of decaying sine-waves when the PFIG is actuated by vibrations in the range of 50-100 mg.

Fig. 8 shows photos of the experimental setup to test and generate a 100 Hz sine-wave with a close-up of the shaker, mount for the PFIG magnet, and disassembled FIG. An example of the generated sine-wave is shown in Fig. 9 with a 220 mV peak. Just as in previous PFIG research a low power op-amp (LMC6484, National Semiconductor) [3] was used to monitor signals where the 1 MΩ oscilloscope load might affect performance (e.g. when measuring V_{Store}). The supplies in Fig. 8 are only there to supply these off-chip op-amps. To produce the vibrations two systems were used. To generate the 100 Hz sine-wave an Unholtz-Dickie model TA30-5 vibration system with a model TA30 250 VA power amplifier was used. To generate the random vibrations ranging between 1-10 Hz an APS Dynamics model 113 shaker with model 125 500 VA power amplifier was used. As described in Section II.A., frequency up-conversion also results in a much higher acceleration on the FIG suspension spring. This is demonstrated by the higher accelerations needed from the Unholtz-Dickie system to produce the tested input voltages. For example, to produce a 220 mV peak input a $\sim$6 g sine-wave vibration is needed, and to produce a 280 mV input a $\sim$7.5 g sine-wave vibration is needed.

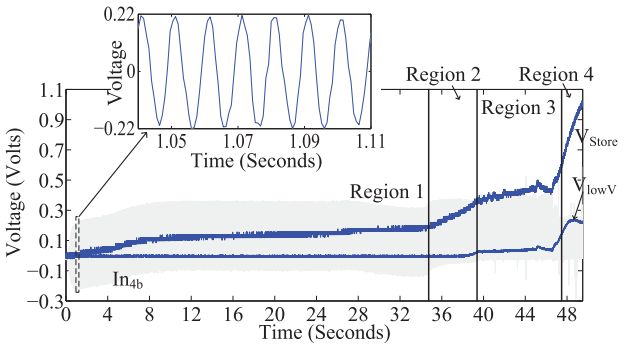

Fig. 9. Experimentally measured charge pump response to a 220 mV sine-wave input. The input into the lowest voltage stage (In_{4b}), the voltage on the lowest voltage stage (V_{lowV}), and V_{Store} are shown. A zoomed-in view of In_{4b} is also shown.

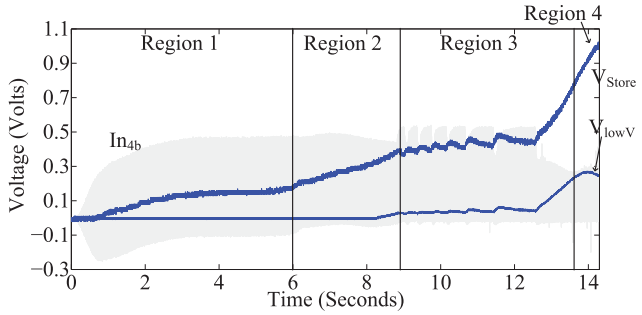

Fig. 10. Experimentally measured charge pump response to a 280 mV sine-wave input.

Efficiency is used to evaluate this circuit once it is out of sub-threshold. Efficiency is defined as the time-averaged circuit output power divided by the time-averaged maximum harvester power in (2). The harvester's maximum power is the power delivered to a matched load (the coil's resistance) over a full input signal period. This means that to determine efficiency with a specific PFIG signal, two measurements are needed. First, the power with the actuated PFIG outputs terminated to a matched load is measured. Second, maximum harvested power is determined with the PFIG actuated by the same vibratory signal using the attached interface circuit.

$$\eta = \frac{\frac{1}{t_2-t_1}\int_{t_1}^{t_2} P_{out-CW}}{\frac{1}{t_2-t_1}\int_{t_1}^{t_2} P_{out-matched\ load}} \tag{2}$$

B. Description of Harvesting Regions

The charge pump interface was tested with a continuum of several different peak input voltages ranging 350 mV to 220 mV. 220 mV represents the lowest peak input voltage that can consistently enable start-up. Based on the behavior and value of V_{Store}, the voltage on the output of the charge pump, four regions of operation can be identified. To better understand and identify these regions Figs. 9, 10, and 11 show experimental data with a peak differential sine-wave input of 220 mV, 280 mV, and 350 mV as well as indicating the four regions of functioning. In Figs. 9, 10, and 11 the input sine-wave into the lowest voltage stage, In_{4b}, is shown in grey. Fig. 9 also shows the zoomed-in view of this sine-wave for a 220 mV input. Fig. 9's low voltage start-up most clearly shows the regions of functioning. The first region represents

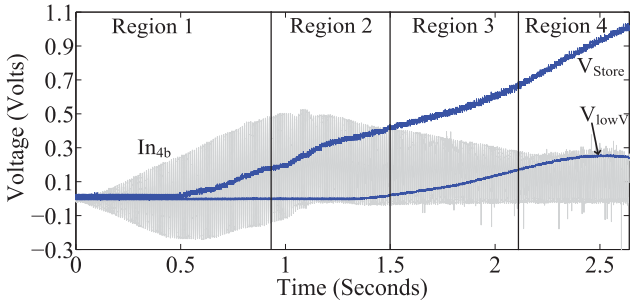

Fig. 11. Experimentally measured charge pump response to a 350 mV sine-wave input.

the slow charging of V_{Store} using passive functioning from 0 V to 0.25 V where the diodes are driven by leakage-based switching. Next, initial active start-up occurs when the comparators and inverters begin to function near 0.25 V, but the voltage on the lowest voltage stage (V_{lowV}) remains near ground. V_{Store} charges quickly here. Third, between 0.4 V and 0.9 V, V_{lowV} begins to rise. Here it is possible for the rise in V_{Store} to become stalled. Lastly, as V_{Store} rises above 0.9 V, it becomes high enough to allow the circuit to be completely biased in saturation.

The similar shape and functioning of the regions can also be seen in Fig. 10; however, much less time is needed for V_{Store} to rise through regions 1 and 3. As the input into the charge pump is higher (e.g. a 350 mV input in Fig. 11), V_{Store} rises quickly and the regions are far more difficult to identify. In Figs. 9, 10, and 11, the input into the comparators, In_{4b}, is initially near its maximum voltage. The interface between the harvester coil and charge pump can be perceived as a voltage divider (Fig. 1). This means the circuit equivalent resistance is high during initial start-up but decreases as the active diodes turn on.

C. Region 1: Passive Leakage-Based Functioning (0-0.25 V)

In a charge pump active diodes increase efficiency and decrease minimum functional voltage by significantly reducing the diode's turn-on voltage. To minimize required cold start-up voltage in the presented charge pump, passive sub-threshold switching (Fig. 12), similar to active diodes, is used. This AC-DC start-up uses the AC harvester output to form signals to reduce the switches' turn-on voltages aiding switching. This passive leakage-based switching on the diode's gates allows start-up from 0 V at voltage levels well below the technology's V_{th} (e.g. minimum start-up at 220 mV and V_{th} at ~400-500 mV). The presented charge pump uses external 100 μF capacitors charged with peak currents >10 μA from cold start.

Fig. 13 shows this initial passive switching on the top PMOS stage in the charge pump, simulated in Cadence, over the first 26 ms of operation with a 350 mV input at 100 Hz. The input voltage, In_{4t}, into the last PMOS is shown in Fig. 13a. V_{Store} rises from 0 V due in part to the current through the top PMOS diode in the grey shaded areas when $T4_{Bar}$ is near ground and $B4_{Bar}$ is high turning on and off the charge pump's last stage diodes (Fig. 13a). The resulting passive switching voltage that turns on the last PMOS device is indicated in Fig. 13a. For comparison, a passive diode's potential turn-on voltage is also indicated in Fig. 13a. Fig. 13b shows how signals Comp T1, B1, and T1 are used to form

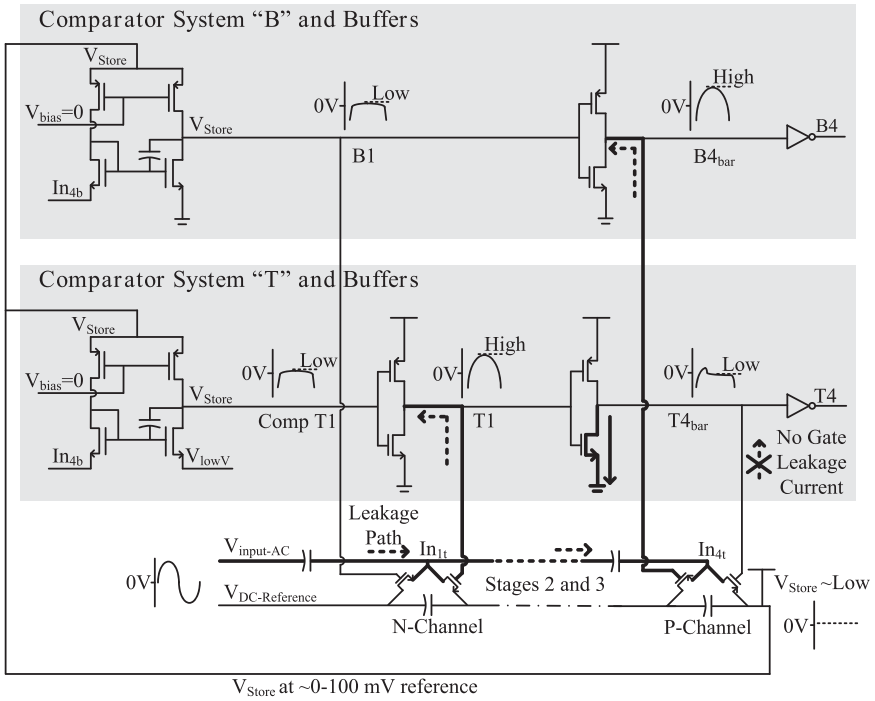

Fig. 12. The AC leakage path in bold is shown on the top part of the full-wave charge pump. The formation of initial passive switching on $T1$, $T4_{Bar}$, $B1$, and $B4_{Bar}$ is shown.

$T4_{Bar}$ and $B4_{Bar}$. The "high" or "low" value of Comp T1, B1, and T1 are indictaed in Fig. 13b. These "high" or "low" voltages lead to the formation of "high" or "low" $T4_{Bar}$ and $B4_{Bar}$ values in Fig. 13a. The leakage-based switching voltage improves upon the potential passive diode voltage. Fig. 13c shows that the peak harvested currents are as high as 25 μA corresponding to In_{4t}'s peak. Even as V_{Store} rises, the passively generated turn-on voltage on the gate of the PMOS diode still goes to ground similar to an active diode. As seen in Fig. 13a, this allows a greater voltage difference and more current flow than if a simple passive diode were between In_{4t} and V_{Store}. The PMOS diode (L = 180 nm and W = 150 μm) will allow some sub-threshold current flow in the $\sim\mu$A range to initially raise V_{Store} from 0 V. As V_{Store} continues to rise in Fig. 13a, more current charges V_{Store} as the PMOS gate voltage is pulled to ground by $T4_{Bar}$.

To form the initial passive switching signals that allow start-up from 0 V, the AC input into the charge pump acts as a supply, rather than V_{Store}, through leakage-based operation. Capacitive leakage over temperature [76], [77] and internal circuit leakage that reduces stored charge must be overcome in storage or switches. However, gate leakage from the AC input can be used to passively switch the active diodes. Fig. 12 shows an example of an AC input's bolded supply path to In_{4t} that produces this passive switching in a portion of the full circuit for signals T1, $T4_{Bar}$, B1, and $B4_{Bar}$. Through this CMOS gate leakage, these gate signals tend to follow In_{4t} unless they are pulled low by the outputs of the respective inverters to which they are attached. The initial peak input gate leakage currents are between ~5-20 pA. This current into node $T4_{Bar}$ decreases as $T4_{Bar}$'s voltage goes low when the inverter's NMOS is pulled down by the high voltage (T1) on the gate of the inverter where $T4_{Bar}$ is an output. The input into this inverter in Fig. 12, T1, follows In_{4t} high. T1 is able to go high because its inverter's input, Comp T1, initially stays low near ground (Fig. 13b). Both lowest voltage stage comparators act as references near V_{Store} (initially near ground). The output of the comparators follow V_{Store} because V_{Bias} is at 0 V for initial start-up. Outputs B2-B4 connected to the comparator output B1 through inverters behave similarly to T1-T4 but with opposite voltages because there is not an extra inverter after their comparator. In this manner, the inverters are initially either pulled low or follow the AC input for all PMOS and NMOS stages switching the charge pump.

MOSFET diodes across the active diodes [43] are not used here. Passive diodes created from the bulk connections are available on the PMOS devices but not the NMOS devices. Simulations in Fig. 13 show that significant current only flows through the switches due to the generated passive gate switching during start-up rather than any added diode. Also, extracted simulations show minimal change in start-up characteristics with and without ESD diodes, indicating that the pad's diodes are not responsible for start-up.

D. Region 2: Sub-Threshold Active Functioning (0.25-0.4 V)

Unlike active sub-threshold rectifier circuits [43], the presented circuit is designed to charge through sub-threshold rather than function in the sub-threshold regime. Active functioning takes over from passive switching when V_{Store} exceeds ~250 mV. The comparators with a V_{Bias} that turns on when V_{Store} is equal to V_{th} were specifically designed for inputs that range from 220-450 mV, so that the comparators would begin to turn on in this region. In this region, the voltage on the lowest voltage stage, V_{lowV}, stays near 0 V. Figs. 9 and 10 show that, following the rise of V_{Store} to ~250 mV, V_{lowV} stays low for ~2-4 seconds before it begins to rise. This is because the

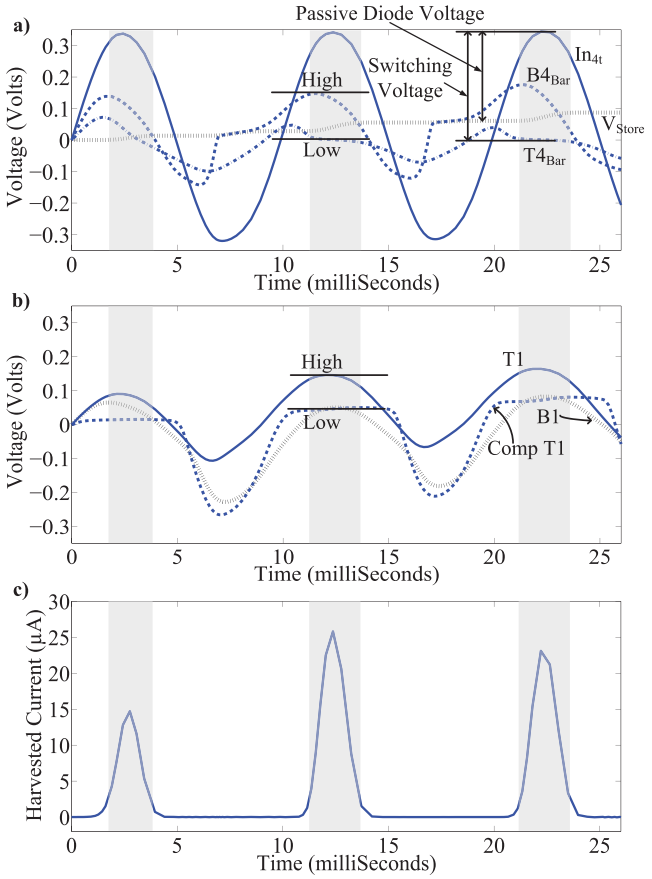

Fig. 13. Simulated charging of V_{Store} over the first 26 milliseconds of operation with a 350 mV peak input at 100 Hz. a) V_{Store}, $B4_{Bar}$, In_{4t}, and $T4_{Bar}$ are shown. b) $T1$, $B1$, and $Comp\ T1$ are shown. c) The current charging V_{Store} through the last PMOS stage is shown.

charge pump stage farthest from the input charges last. This architecture uses this uneven charging to aid in start-up. Active diode switching based on the lowest voltage stage comparator, with one input near 0 V, enables a higher V_{gs} in the comparator. Also, the input near 0 V means more time in a cycle for sub-threshold current to cause the comparators to switch.

Fig. 14 shows an example of the transition point during a small window of time (e.g. after t = 1.5 seconds in Fig. 11) during active start-up. The comparators in sub-threshold are set to switch (the transition point) when the input into the lowest voltage stage (In_{4b}) exceeds V_{lowV} (near 0 V). This transition point is below the average level of charging per stage (~60 mV in Fig. 14) throughout the charge pump. Fig. 14 also indicates the clocking level when the comparators switch. Switching based on the difference between V_{lowV} and In_{4b} creates a greater V_{gs} in the comparator, minimizing the delay between the transition point and the time when the clock switches. This ~1 ms delay is still large (Fig. 14), and it reduces charging. It would be larger if the comparator decisions were not made from the lowest voltage stage. However, the advantage of driving the comparators from the lowest voltage stage can diminish as V_{Store} and correspondingly V_{lowV} rise.

E. Region 3: Mid-Level Active Functioning (0.4-0.9 V)

As V_{Store} rises past 0.4 V, there is the possibility of stalling. This section describes this stalling and solutions to mitigate it.

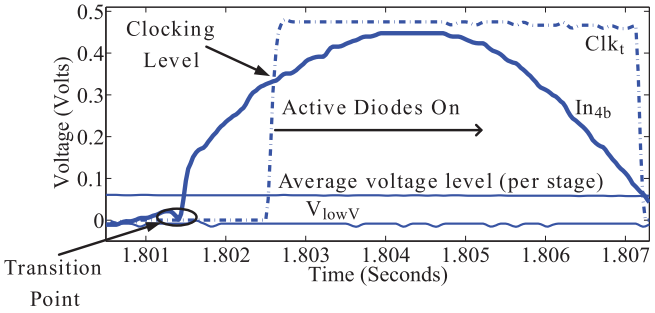

Fig. 14. Experimentally measured circuit start-up with a 350 mV input sine-wave over a narrow window of time. The transition point, the average voltage level per stage, and the clocking signal are indicated.

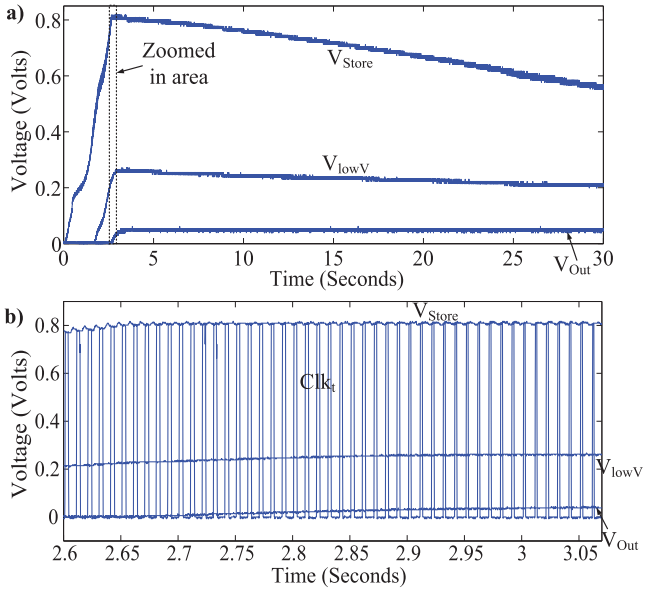

Fig. 15. a) Experimentally measured results with a 350 mV sine-wave input. V_{Store}, V_{Out} and V_{lowV} are shown when the mode selector turns on near 0.8 V and charging stalls. b) A close up of the failure is shown with Clk_t also plotted.

Fundamentally, as V_{Store} rises to ~400 mV, V_{lowV} begins to rise and the additional V_{gs} used to switch the system described Fig. 14 is lost. Start-up to ~400 mV is possible at voltages lower than 220 mV. However, to boost over 1 V, a minimum peak input of 220 mV at ~100 Hz is necessary to overcome stalling in this region (region 3). For instance, in Figs. 9 and 10 V_{Store} has difficulty rising past 0.5 V. The mode selector helps prevents this stalling and is described here. The effect on start-up when using a PFIG actuated with non-periodic bridge-like vibrations will also be discussed. This discussion will include an explanation of why 100 μF capacitors throughout the charge pump may aid start-up when the input is non-periodic.

First, consider the case of the mode selector set for ~0.8 V output, with a 350 mV unloaded peak input sine-wave. Fig. 15a shows V_{Store}, V_{Out}, and V_{lowV}. The charge pump stalls when V_{Store} reaches 0.8 V; the circuit cannot maintain this value. At this point, V_{Out}, attached to a 100 μF capacitor connected to ground, rises to ~0.1 V while V_{lowV} rises to ~0.25 V. The charge pump stalls because V_{lowV} is too high relative to V_{Store}. There is not a large enough V_{gs} to pull down the NMOS connected to V_{lowV} in the comparator (Fig. 6) when V_{Store} is at 0.8 V with the comparator still in sub-threshold.

With a 100 μF capacitor attached to V_{Out}, V_{Store} cannot rise relative to V_{lowV}'s rise. In Fig. 15b, a zoomed in view of the stalling shows that as V_{lowV} rises, the clock outputs become narrow. The clock outputs will be unable to properly switch the active diodes, stalling the charging process.

Raising the input voltage level will help to avoid stalling. Also, stalling can be avoided by raising the voltage at which the mode selector turns on so that V_{Store} will be higher relative to V_{lowV} during the sub-threshold charging process. In other words, a higher mode selector turn-on voltage keeps the transition point (Fig. 15) low relative to V_{Store} for a longer period during start-up. Aside from the mode selector, an external capacitor and resistor to ground on V_{lowV} can slow its rise and aid start-up (e.g. R = 20 kΩ and C = 5.7 μF). For example, start-up was possible with ease using a 240 mV input as long as similar values of R and C were used between V_{lowV} and ground. However, 20 kΩ and 5.7 μF were necessary to achieve a repeatable start-up at 220 mV. A lock-up condition is possible where more voltage is necessary for start-up than originally required if the voltage on V_{lowV} becomes too high during stalling. This motivates evaluation with non-periodic inputs.

This region of operation was examined with the PFIG actuated using both periodic and non-periodic (bridge-like) vibrations. When the PFIG was actuated with a periodic 4.5 Hz input, a minimum peak of 415 mV with average input power of ~9 μW was required for start-up. Start-up is also possible for PFIG actuation with non-periodic bridge-like vibrations. The accelerations applied range between 30-100 mg (Fig. 16a). The open circuit PFIG peak output only occasionally exceeds 415 mV here. All capacitors were discharged before this test. Measured voltages V_{Store}, V_{lowV}, and the loaded FIG output are shown in Fig. 16b. A zoomed-in example of an up-converted sine-wave input generated by the PFIG in Fig. 16b is shown in Fig. 16c. With a matched FIG output, the bridge-like acceleration pattern produces ~8.5 μW of circuit output power over 20 seconds. Bursts of higher acceleration PFIG actuations (shaded in grey in Fig. 16a) starting near 11 seconds allow V_{Store} to rise past ~0.5 V without stalling. Higher power is only needed during the weak point of start-up (0.4-0.9 V). After this the charge pump is able to transition to full active functioning with high power efficiency.

The need for large 100 μF capacitors throughout the charge pump can also be explained by examining Fig. 16b. For example between ~8.5 and ~9.5 seconds, the PFIG is actuated only once. Periods with little to no actuation like this are inevitable when a harvester is actuated by traffic-based bridge vibrations. Instead of 100 μF capacitors, consider using capacitors that are less than 1 μF. The current necessary to charge these capacitors will be significantly less, and this may begin to decrease the turn-on voltage of the charge pump similar to vibration harvesting research [57] or even RF research [51]. The problem is that, when using 1 μF capacitors during this active start-up, the circuit itself will consume the charge stored in the capacitors throughout the charge pump if actuations don't occur frequently. This will cause V_{Store} to decrease quickly. This is a potential reason why research into cold start-up that decreases a diode's turn-on without just reducing the current through the diode is so valuable.

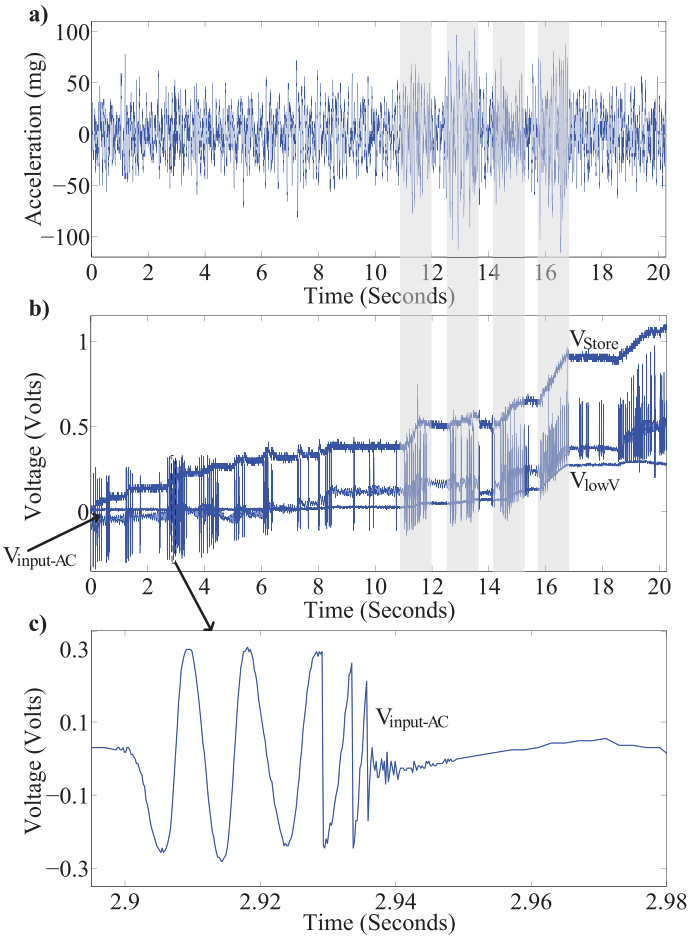

Fig. 16. Experimentally measured start-up is demonstrated with non-periodic bridge-like vibrations harvested using a PFIG. a) Measured acceleration is shown. b) The measured PFIG output into the charge pump along with the circuit voltages V_{lowV} and V_{Store} are shown. c) A zoomed-in view of the PFIG output is shown.

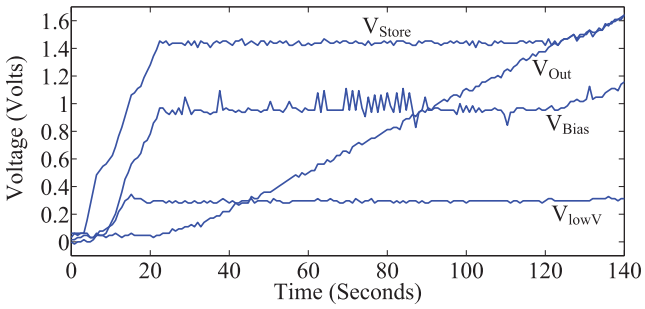

Fig. 17. Experimentally measured results using a PFIG input signal with a 450 mV peak show start-up. The lowest voltage stage (V_{lowV}), V_{Bias}, V_{Store}, and V_{Out} are shown.

F. Region 4: Full Active Functioning (>0.9 V)

Once V_{Store} exceeds ~0.9 V, steady-state functioning is possible without stalling. For example, in Fig. 17 V_{Store} stays at ~1.45 V for ~100 seconds as V_{Out} (attached to a 100 μF capacitor connected to ground) charges from 0 V. There is no stalling because the system is out of sub-threshold, and V_{Bias} is well above ground. In this region, reasonably high efficiency is demonstrated with a PFIG. For a 7.6 μW input from a PFIG actuated at 3 Hz with a peak of 450 mV the measured circuit efficiency was ~50% (V_{Out} > 1.2 V).

TABLE I
COMPARISON OF RELEVANT VIBRATION HARVESTING RESEARCH

Research	Input Description	Technology	Architecture	Start-up Voltage*	Efficiency	Load
This Work	$\sim$5μW-20μW Non-periodic	180nm CMOS	Charge Pump	220mV	$\sim$50%	100μF
[34]-Du	34.4μW Non-periodic Piezo	350nm HV CMOS	LC Converter	$\sim$800mV	NA	5.2mF
[78]-Cassidy	$\sim$5W Non-periodic/stochastic	3-Phase Electronics	LC Converter	$\sim$6V	NA	$\sim$1Ω
[67]-Ulusan	$\sim$32μA Periodic	180nm CMOS	Charge Pump	400mV	$\sim$38%	4.4MΩ
[66]-Ulusan	$\sim$60μA Periodic	90nm CMOS	Charge Pump	400mV	$\sim$67%	47μF
[57]-Singh	Periodic	180nm CMOS	Charge Pump	$<$100mV	NA	150 pF
[43]-Peters	Periodic	350nm CMOS	Voltage Doubler	380mV	$\sim$90%	10μF
[65]-Leicht	2.6μW-1.2mW Periodic	350nm CMOS	LC Converter	570mV	$\sim$95%	47μF
[17]-Cheng	$\sim$mW Periodic	Discrete Electronics	Charge Pump	500mV	$>$80%	220μF
[4]-Galchev	$\sim$1μW-2μW Non-periodic	Schottky Diodes	Charge Pump	$\sim$300mV	$\sim$10%	10μF
[70]-Rao	$\sim$960μW Non-periodic	500nm CMOS**	Rectifier	400mV	$\sim$87%	$\sim$7.5kΩ
[3]-McCullagh	$\sim$5μW-20μW Non-periodic	Schottky Diodes	Transformer	$\sim$50mV	$\sim$38%	10μF
[44]-Maurath	40μW Periodic	350nm CMOS	Charge Pump	NA***	$\sim$50%	100μF
[68]-Herbawi	$\sim$32μA Periodic	350nm CMOS	Rectifier	500mV	$\sim$95%	1μF
[47]-Szarka	200μW Periodic	Discrete Electronics	LC Converter	500mV	$\sim$51%	$\sim$420Ω
[6]-Guilar	Multi-frequency Periodic	350nm CMOS	Rectifier	$\sim$400mV	$>$90%	$\sim$1kΩ
[69]-Wang	54.5mW Periodic	Schottky Diodes	LC Converter	$\sim$400mV	$\sim$71%	$\sim$300Ω

*Input voltages are peak AC unless otherwise noted
**Schottky diodes are also used
***An 800mV DC pre-charge is needed

Various losses decrease efficiency. In (1) optimal efficiency is predicted to be between 200-300 mV. As the FIG output is similar to a decaying sine-wave, perfect optimization for efficiency will not be possible. Rather, the charge pump should be optimized for a typical peak voltage. Efficiency losses include active power. Active power was measured with V_{Store} between 1-1.5 V by adding a resistor after V_{Store} to measure $\sim$0.6 μW without PFIG actuation. This power level was verified in simulation where high frequency (10 Hz) PFIG outputs increase power to $\sim$1 μW. Other active boosting circuits [16], [17], [47], [63] give higher efficiencies but consume $>$5 μW active power. Another source of efficiency loss is that the active diode switching is lined up with only the lowest voltage stage because of small delays through the 100 μF capacitors.

IV. CONCLUSION

The charge pump presented here offers low power ($\leq\sim$1 μW) rectification and boosting of low voltage (220 mV) AC inputs to $\sim$1-1.5 V DC charging 100 μF capacitors from cold start. The use of large 100 μF capacitor throughout the charge pump architecture is an advantage and a goal of this design. These large capacitors potentially allow a stable start-up with non-periodic inputs. Periodic and non-periodic inputs generated on a shaker table show the circuit's capabilities and limitations (e.g lock-up and stalling in region 3). With only one input the presented circuit functions as the supply voltage rises from cold start using both unique passive and sub-threshold active functioning without a transformer or pre-charged supply.

Table I compares the presented circuit's characteristics to relevant state-of-the-art vibration energy harvester systems. Most of the circuits built for vibration energy harvesters focus on periodic inputs. However, some systems and circuits are designed to address a specific aspect of a non-periodic input. For example, electronics for high-power high-voltage 3-phase energy harvesters focus on optimal control techniques for non-periodic (specifically stochastic) inputs [78], [79] where start-up is not a concern. Other IC research focuses on combining the signals for multiple harvested resonant frequencies [6]. Previous circuit research for the PFIG focused on start-up with low-power low-voltage inputs. However, it did not use ICs and instead used technologies such as transformers [3] or Schottky diodes [4]. Using small ($\sim$150 pF capacitors) for storage in a charge pump will reduce start-up voltage [57], but this does not meet the requirements of many bridge health monitoring systems (e.g. [21]). Also, it would not work when using an active diode charge pump with non-periodic inputs where input power could significantly reduce in the middle of start-up.

Advanced integrated circuit solutions exist to boost and rectify vibration harvests inputs as low as 40 μW, but a pre-charged supply is needed [44]. Compared to previous IC (or combined discrete and IC) research that rectifies and boosts from cold start [16], [17], [43], [47], [65]–[70] the presented research's unique architecture using only two comparators and leakage-based start-up has many advantages. Power and turn-on voltage are reduced and this results in a significantly reduced cold start-up voltage. The presented circuit's efficiency is 50% with PFIG inputs, and its eight-stage CW charge pump architecture uses only $\sim$1 μW of power. The presented circuit is the best option for start-up and harvesting from a non-periodic vibration harvester with a low-voltage low power input. Additionally, it lays the framework for further research where a low frequency input and large off-chip capacitors are used with an integrated circuit control to reduce turn-on voltages and required power.

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